IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 11, Issue 2 Ver. I (Mar. – Apr. 2016), PP 86-91
www.iosrjournals.org

THD Minimization of 3-Phase Voltage in Five Level Cascaded H-Bridge Inverter

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Abstract*: In this paper, the analysis of Selective Harmonic Elimination (SHE) for 3-Phase Voltage Source Inverter (VSI) is presented. Investigation harmonics which are produced by Pulse Width Modulation (PWM) technique is necessary as it affects the system parameters. Higher order harmonics are easily eliminated by choosing a proper tuned value filters but lower order harmonics such as 3rd, 5th, 7th, and 9th are not eliminated easily. This paper presents optimization method for SHE reduction i.e. Newton Raphson Method with random initial guess and shows the various feasible regions where the solution can exit by solving transcendental non linear equations. .By using this method lower order harmonics as well as Total Harmonic Distortion (THD) will also reduce. In this paper a cascaded 3-Phase, 5- Level, H-bridge Multilevel Inverter using MATLAB/Simulink blocks is presented as a systematic approach for developing the model.*

Keywords*: Flexible AC Transmission System, Multilevel Inverter, Power Electronics, Selective Harmonic Elimination, SPWM-Sinusoidal Pulse Width Modulation*

I. Introduction

Recently Multilevel Inverters are widely used in many industrial applications, where the requirement is medium voltage and high power applications. Multilevel Inverter has been widely used for chemical, oil, and liquefied natural gas plants, water plants, marine propulsion, power generation, energy transmission, and power-quality devices, FACTS Devices [1-3]. Cascaded H-bridge converter topology is prominently used and particularly useful for renewable energy and DSTATCOM applications [4-5], [9]. While in comparison with traditional two-level voltage source inverters, multilevel inverters have several advantages. The main advantage of multilevel inverter is that of its stepwise output voltage. This advantage results in higher power quality, lower switching losses, higher voltage capability moreover it also reduces the cost with transformer less system at the distribution side. It has low distortion, low dV/dt and can draw input current with very low distortion, can generate smaller common mode voltage, thus reducing the stress in the motor bearings in motor applications, and also it can operate with a lower switching frequency. Desired output can be obtained from multilevel inverter with several number of dc voltages as inputs. If the number of levels is increased the output voltage and current waveform approaches to the sinusoidal waveform. The different topologies, control strategies and modulation techniques used for Multilevel inverters have been presented in [6-7]. Reference [8] elaborates the industrial applications of multilevel inverter. Consequently the reduced switching methods with lower computation cycles are investigated in [10].

The generalized formulation of Selective Harmonic Elimination of multilevel inverter is presented in literature recently. Half wave symmetry SHE PWM formulation is presented in [11-14], which describes the formulation of SHE problem based on lower harmonic elimination technique. The generalized problem for SHE is presented in various papers and nonlinear equations with advanced computing methods like genetic algorithm, particle swarm optimization, bee algorithm and bacterial foraging [13-17]. These papers primarily focus on the method of solving the nonlinear equations with the exact formulation of SHE problem with MATLAB/Simulink. resent paper attempts to formulate the in depth MATLAB/Simulink based simulation of SHE problem with optimization algorithm that will help the new researchers to carry out the research for further investigating new SHE algorithms by spending less time in modeling the SHE problem.

II. Review Of Generalized She For Multilevel Inverter

The A multilevel cascade inverter consists a number of H-bridge cells that are connected in series per phase, and each module requires a separate DC source to generate voltage levels at the output of inverter.

$$V_{out} = \begin{cases} V_{dc} & In_1, In_4 \text{ ON} \\ 0 & In_1, In_3 \text{ ON} \\ -V_{dc} & In_2, In_3 \text{ ON} \end{cases} \qquad (1)$$

The switching inputs shown as S_i, i=1 to 4 in the Fig. 1 allows obtaining output voltage as per (1). The H-bridge cells are serially connected over AC outputs to obtain expanded phase voltage levels and therefore, the total output level is the synthesize of cells output of each H-bridge. Cascade Multilevel Inverter (CMLI) is one of the most important topology in the family of multilevel and multipulse inverters.

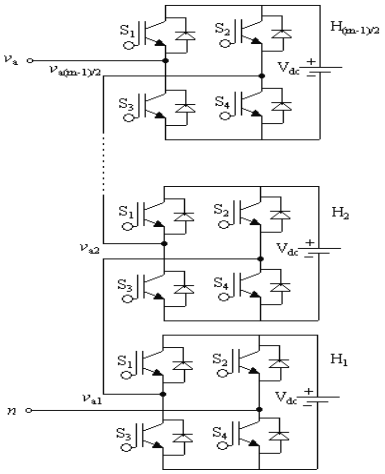

Fig.1 Cascaded H-Bridge Multilevel Inverter

It requires least number of components as compared to diode-clamped and flying capacitors. The minimum number of levels and the voltage rating of the active devices (IGBTs, GTOs, power MOSFETs, etc.) are inversely related to each other. More levels in the inverter will lower the required voltage device rating of individual devices; or looking at it another way, a higher voltage rating of the devices will enable a fewer minimum number of levels to be used. The cascaded multilevel inverter consists of a number of H-bridge inverter units with separate dc source for each unit and is connected in cascade or series as shown in Fig. 1.

The output voltage levels as seen from Fig. 2 of each phase and each line voltage is given by (2) and (3) respectively.

$$m = 2s + 1 \quad (2)$$

$$\text{Switching devices} = 2(m-1) \quad (3)$$

$$\text{DC Bus capacitors} = (m-1)/2$$

where 's' is the number of bridges, 'm' is the number of levels. The ratio of DC voltage source naturally affects the output levels of a cascade multilevel inverter. The Fourier series expansion of the general multilevel stepped output voltage is given in (4), where n is the harmonic number of the output voltage of inverter.

$$V(wt) = \sum_{n=1}^{\infty} Vn \sin(nwt) \quad (4)$$

Where

$$V(n) = \frac{4Vdc}{n\pi} \sum_{n=1}^{\infty} \begin{cases} \cos(n\theta i) & \text{for odd ns} \\ 0 & \text{for even ns} \end{cases}$$

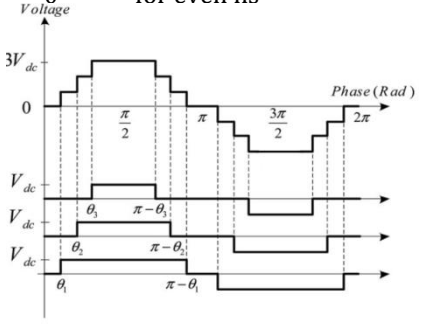

Fig. 2 Output voltage waveform of 7-level Cascaded Multilevel Inverter

The switching angles can be chosen to obtain minimum voltage harmonics. Normally, these angles are chosen so as to cancel the predominant lower frequency harmonics. The selective harmonic elimination method is also called fundamental switching frequency method based on the harmonic elimination theory proposed in [18],[19]. The major difficulty for selective harmonic elimination methods, including the fundamental switching

frequency method and the Virtual Stage PWM method, is to solve the transcendental equations for switching angles.

To satisfy fundamental voltage and to eliminate 5th and 7th harmonics, three nonlinear equations are as follows.

$$V_1 = \frac{4Vdc}{\pi}\left[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3)\right] = V_1^* \qquad (5)$$

$$V_5 = \frac{4Vdc}{5\pi}\left[\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3)\right] = 0 \qquad (6)$$

$$V_7 = \frac{4Vdc}{7\pi}\left[\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3)\right] = 0 \qquad (7)$$

$$\text{Subject to } 0 < \theta_1 < \theta_2 < \theta_3 < \frac{\pi}{2}$$

These equations are nonlinear transcendental equations are solved by Newton-Raphson method using Random Initial Guess, as the solution doesn't depend upon the guess. This paper presents a multilevel inverter model with mathematical model for SPWM modulator to minimize THD.

III. Description Of Model For Case Study Of 5-Level Inverter

The primary building blocks in MatLab can be divided into 3 subsystems namely: Generation of gate pulses, simulation of 5-level inverter by spwm method, minimization of harmonics and THD by selective harmonic elimination method.The Reference sine wave is generated sine block with 120° displacement for each phase and amplitude as per the modulation index requirement. Fig. 3 shows the phase and line voltage of 5-level multilevel inverter whereas Fig.4 shows the FFT analysis showing Total THD of 71.20% by SPWM method.

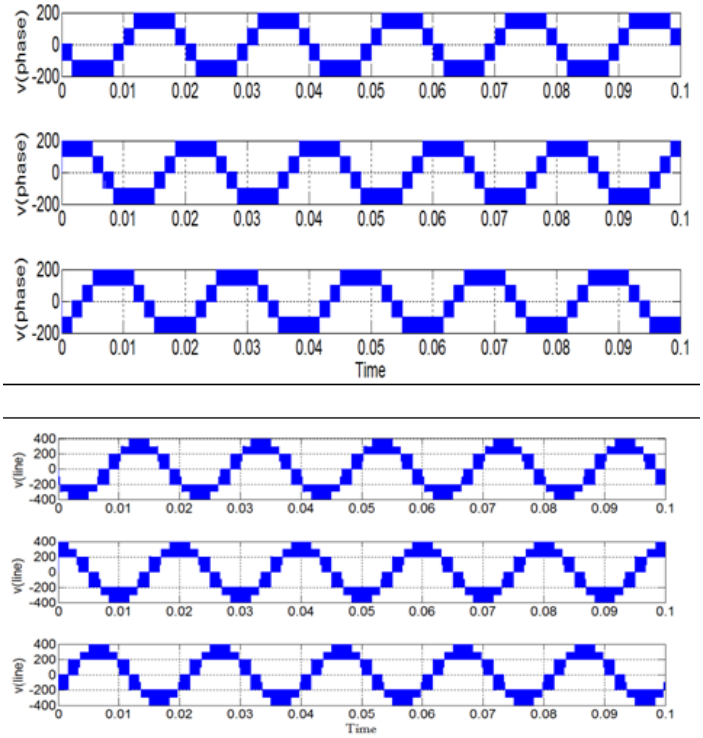

Fig. 3 Phase & Line Voltages of 5 Level Inverter

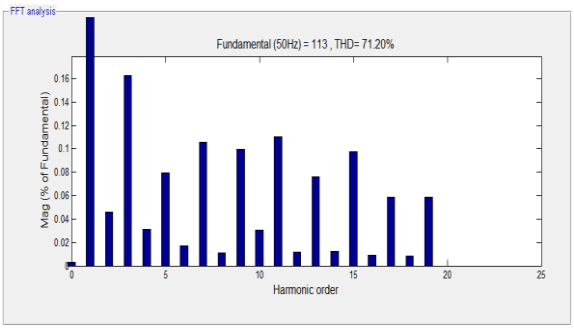

Fig. 4 FFT Analysis by SPWM Method

IV. Selective Harmonic Elimination Method

These offline calculated constant values of firing angles are then compared with the sine wave through comparator and given to gate pulses of respective switches(IGBT) in H- Bridge Model. For three phase generation the angles are displaced by 120° in each phase. The corresponding system for generating firing pulses is shown in Fig. 5. The dead band is not considered in this simulation model and complementary pulse is fed to the upper and lower switches of each leg of H bridge inverter. Here sine wave is compared with firing angle

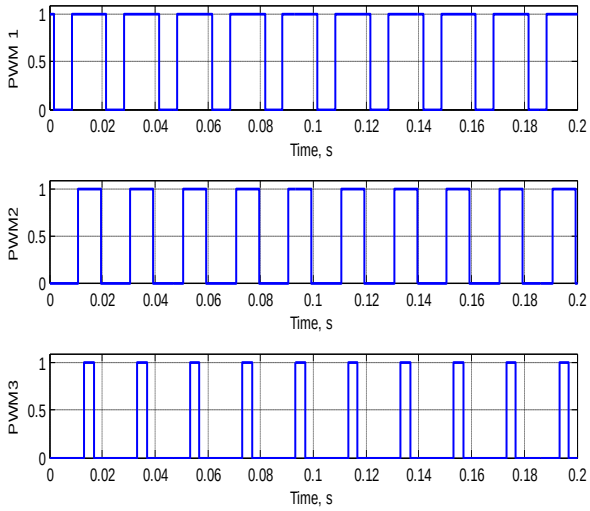

Fig. 5 PWM Pulses for generating H bridge

By inserting notches at a particular instant, total THD is reduced to 4.66% which is below IEEE 519 standard as shown in Fig.6

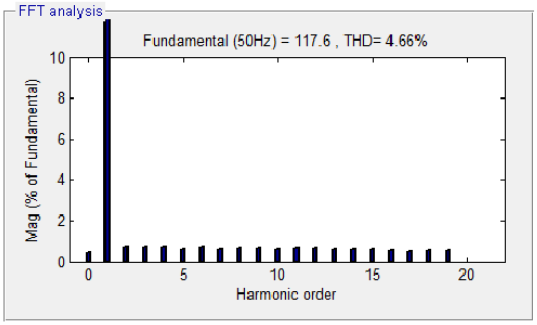

Fig. 6 FFT Analysis for Selective Harmonic Elimination (SHE)

S. No	Harmonic Elimination Techniques	FFT Analysis of Magnitude (% of fundamental)	Total Harmonic Distortion (THD)
1	Sinusoidal PWM Technique	113.3	71.20
2	Selective Harmonic Elimination Technique	117.6	4.66%

V. Filter Section

Here LC filter is used to filter out the ripple and minimize the higher order harmonics In LC filter an Inductor is connected in series with the load (RL). It offers high resistance path to The load (RL). The capacitor transverse the load through the inductance, In this manner the AC component are filtered and a flat

DC is supplied all the way through the load. Here the distorted harmonics are removed and the smooth wave forms are obtained .Here the distorted harmonics are removed and the smooth wave forms are obtained as shown in Fig. 7 & 8.

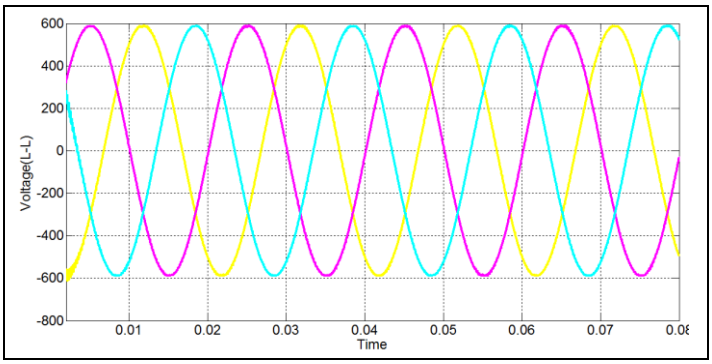

Fig. 7 Line Voltage of 5 Level Inverter

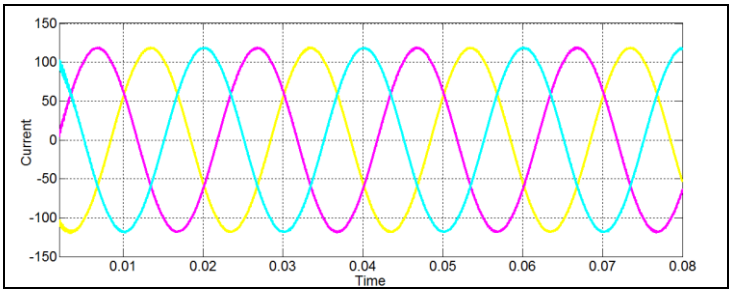

Fig. 8 Line Current of 5 Level Inverter

VI. Conclusion

Simulation of Multilevel Inverter for three phase 5-Level inverter with SHE in MATLAB/Simulink is presented as a systematic design approach. The results obtained from simulation of MATLAB/Simulink shows that the harmonic THD contents are 4.66% and also third, fifth and seventh harmonics are within 1% tolerance. 9^{th} harmonic shall be automatically cancelled and other higher order harmonics are eliminated by filter. While it is to be noted that the fundamental harmonic is preserved and selected order of harmonics are very small which strongly confirms the validity of proposed system.

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